Claim Amendments

1. (Currently Amended) A method comprising:

using a logic design element in a logic design;

performing a simulation of the logic design that includes simulating the logic design element; and

having the logic design element automatically collect and store instrumentation data during the simulation, wherein the instrumentation data represents usage and performance related statistics that relate to the logic design element~~.~~;

wherein the logic design element represents a FIFO memory, and

the instrumentation data collected by the logic design element comprises a degree of fullness of the FIFO memory.

2. (Original) The method of claim 1 further comprising displaying the instrumentation data relating to the logic design element.

3. (Original) The method of claim 2 further comprising receiving a query to display the instrumentation data relating to the logic design element, wherein displaying the instrumentation data includes displaying the instrumentation data relating to the logic design element in response to the query.

4. (Original) The method of claim 2 wherein displaying the instrumentation data includes displaying the instrumentation data after performing the simulation.

5. (Original) The method of claim 2 wherein displaying the instrumentation data includes displaying the instrumentation data while performing the simulation.

6. (Original) The method of claim 2 wherein:

performing the simulation includes performing a partial simulation,

having the logic design element automatically collect the instrumentation data includes having the logic design element automatically collect the instrumentation data during the partial simulation, and

displaying the instrumentation data includes displaying the instrumentation data after performing the partial simulation.

7. (Canceled).

8. (Currently Amended) The method of claim ~~7~~ 1 wherein having the FIFO memory automatically collect the instrumentation data includes having the FIFO memory record usage of the FIFO memory during the simulation.

9. (Currently Amended) The method of claim ~~7~~ 1 further comprising:

receiving a query to display the instrumentation data relating to the FIFO memory, and

displaying the instrumentation data relating to the FIFO memory in response to the query.

10-12. (Canceled).

13. (Currently Amended) A ~~machine-accessible medium~~ computer readable storage medium storing instructions which when accessed results in a machine performing operations comprising:

using a logic design element in a logic design;

performing a simulation of the logic design that includes simulating the logic design element;

having the logic design element automatically collect instrumentation data during the simulation, wherein the instrumentation data represents usage and performance related statistics that relate to the logic design element; and

displaying the instrumentation data relating to the logic design element~~.~~ ;

wherein the logic design element represents a tri-state bus, and

the instrumentation data collected by the logic design element comprises a number of occurrences of bus error conditions experienced by the tri-state bus.

14. (Canceled).

15. (Currently Amended) The ~~machine-accessible~~ computer readable storage medium of claim 13 further comprising receiving a query to display the instrumentation data relating to the logic design element, wherein displaying the instrumentation data includes displaying the instrumentation data relating to the logic design element in response to the query.

16. (Currently Amended) The ~~machine-accessible~~ computer readable storage medium of claim 13 wherein displaying the instrumentation data includes displaying the instrumentation data after performing the simulation.

17. (Currently Amended) The ~~machine-accessible~~ computer readable storage medium of claim 13 wherein displaying the instrumentation data includes displaying the instrumentation data while performing the simulation.

18. (Currently Amended) The ~~machine-accessible~~ computer readable storage medium of claim 13 wherein:

performing the simulation includes performing a partial simulation,

having the logic design element automatically collect the instrumentation data includes having the logic design element automatically collect the instrumentation data during the partial simulation, and

displaying the instrumentation data includes displaying the instrumentation data after performing the partial simulation.

19-22. (Canceled).

23. (Currently Amended) The ~~machine-accessible~~ computer readable storage medium of claim ~~22~~ 13 wherein having the tri-state bus automatically collect the instrumentation data includes having the tri-state bus automatically collect usage of the tri-state bus during the simulation.

24. (Currently Amended) The ~~machine-accessible~~ computer readable storage medium of claim ~~22~~ 13 further comprising:

receiving a query to display the instrumentation data relating to the tri-state bus, and

displaying the instrumentation data relating to the tri-state bus in response to the query.

25-31 (Cancelled)

32. (Currently Amended) The ~~machine-accessible medium~~ method of claim ~~13~~ 1 wherein

~~the logic design element represents a FIFO memory, and~~

the instrumentation data collected by the logic design element comprises statistics regarding usage of the FIFO memory.

33. (Currently Amended) The ~~machine-accessible medium~~ method of claim ~~13~~ 1 wherein

~~the logic design element represents a FIFO memory, and~~

the instrumentation data collected by the logic design element comprises a percentage of time a word of the FIFO memory was in use.

34. (Currently Amended) The machine accessible medium of claim 13 wherein

~~the logic design element represents a tri-state bus, and~~

the instrumentation data collected by the logic design element comprises a number of simulation cycles a tri-state bus driver drove the tri-state bus.

35. (Currently Amended) The ~~apparatus~~ method of claim ~~25~~ 1 wherein

~~the logic design element represents a FIFO memory, and~~

the instrumentation data collected by the collection module of the logic design element comprises a quantity of valid entries present in the FIFO memory during the simulation.

36. (Currently Amended) The ~~apparatus~~ method of claim ~~25~~ 1 wherein

~~the logic design element represents a FIFO memory, and~~

the instrumentation data collected by the collection module of the logic design element comprises a quantity of read and write pointers used by the FIFO memory during the simulation.

37. (Cancelled)